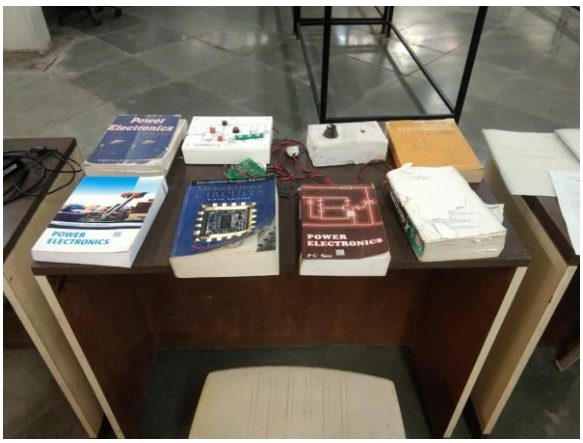
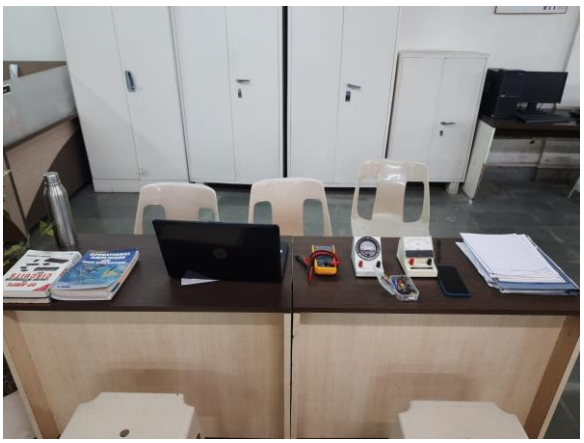
Glimpses of the Festival of Examination

Group Discussion

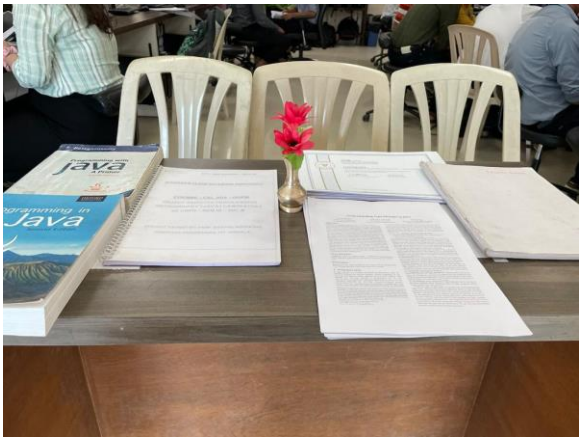
Top-down approach



Choice based approach



Open resource approach



Reverse problem methodology

Choice based approach

VIT Vidyalankar Institute of Technology
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Version 0120-7

Consolidated Academic Administration Plan for the Course

_____(mention elective / core as per NBA) Sem. _____ – Program _____ 2021-2022 –Even Semester

Faculty - Prof. _____(Cluster Mentor) & Prof. _____

The academic resources available in VIT –

VMIS (ERP)	V-Refer and V-Live	VIT Library	VAC & MOOC Courses
Institute & Department Vision and Mission	Former IA question papers and solutions (prepared by faculty)	Former IA question papers solutions - hardcopy	Value Added Courses (VAC) are conducted throughout the semester & in the semester break - Enrol for the VACs
Program Educational Objectives (PEO)	MU end semester examination question papers and solutions (prepared by faculty)	MU end semester exam question paper & solutions - by faculty, hardcopy	
Program Specific Outcome (PSO)	Class notes and Digital Content for the subject (scanned / typed by faculty)	All text books, reference books, e -books mentioned in the syllabus & AAP	Online courses from NPTEL, Coursera etc. are pursued throughout the semester - Register for the course & get certified
Program Outcome (PO)	Comprehensive question bank, EQ, GQ, PPT, Class Test papers	Technical journals and magazines for reference	
Departmental Knowledge Map	Academic Administration Plan & Beyond Syllabus Activity report	VIT library is member of IIT Bombay Library	Watch former lectures captured in LMS at VIT

1.a Course Objectives (Write in detail – as per NBA guidelines)

Cognitive	What do you want students to know?	
Affective	What do you want students to think / care about?	
Behavioural	What do you want students to be able to do?	

Advice to Students:

Attend every class!!! Missing even one class can have a substantial effect on your ability to understand the course. Be prepared to think and concentrate, in the class and outside. I will try to make the class very interactive. Participate in the class discussions. Ask questions when you don't understand something. Keep up with the class readings. Start assignments and homework early. Meet me in office hour to discuss ideas, solutions or to check if what you understand is correct. The v-Refer Link for this course (**Creation of microsite (vit.edu.in or teams) e.g. https://cs50.harvard.edu/college/2021/spring/)**

Collaboration Policy:

We encourage discussion between students regarding the course material. However, no discussion of any sort is allowed with anyone on the assignment and homework for the class. If you find solution to some problems in a book or on the internet, you may use their idea for the solution; provided you acknowledge the source (name and page in the book or the website, if the idea is found on the internet). Even though you are allowed to use ideas from another source, you must write the solution in your own words. If you are unsure whether or not certain kinds of collaboration is possible please ask the teacher.

1.b Course Outcome (CO) Statements and Module-Wise Mapping (follow NBA guideline)

CO No.	Statements	Related Module/s
CO1		
CO2		
CO3		
CO4		
CO5		

1.c Mapping of COs with POs (mark S: Strong, M: Moderate, W: Weak, Dash '–': not mapped)

(List of POs is available in V-refer)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1												
CO 2												
CO 3												
CO 4												
CO 5												

1.d Mapping of COs with PSOs (mark S: Strong, M: Moderate, W: Weak, Dash '–':not mapped)

	PSO 1	PSO 2	PSO 3	PSO 4
CO 1				
CO 2				
CO 3				
CO 4				
CO 5				

1.e Teaching and Examination Scheme (As specified by the University) for the Course

Categories	Mathematics	Basic Science & General Engg.	Humanities & Soft Skill	Core Engg./ Technology - Design & Analysis	Multidisciplinary
Tick suitable category					

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
(For Theory Only)			-			-		
(For Lab Only)		-			-			

Subject Code	Subject Name	Examination Scheme							
		Theory Marks IA Test			End Sem. Exam Marks	TW	Practical	Oral	Total
		IA 1	IA 2	Average of IA1 and IA2					
(For Theory Only)									
(For Lab Only)									

1.f Faculty-Wise Distribution of all Lecture-Practical-Tutorial Hours for the Course

Divisions	Lecture (Hrs.)	Practical (Hrs.)				Tutorial (Hrs.)			
		Batch 1	Batch 2	Batch 3	Batch 4	Batch 1	Batch 2	Batch 3	Batch 4
A									
B									
C									

1.g Office Hours (Faculty will be available in office in this duration for solving students' query)

Division	Day	Time (at least 1 Hr. / Division)	Venue (Office Room No.)
A			
B			
C			

2.a Syllabus : Module Wise Teaching Hours and % Weightage in University Question Paper

Module No.	Module Title and Brief Details	Teaching Hrs. for each module	% Weightage in University Question Papers
1			
2			
3			

4			
5			
6			
* Insert rows for more modules in the Course	**Total**		

2.b Prerequisite Courses

No.	Semester	Name of the Course	Topic/s
1			
2			
3			

2.c Relevance to Future Courses

No.	Semester	Name of the Course
1		
2		
3		

2.d Identify real life scenarios / examples which use the knowledge of the subject

Real Life Scenario	Concept Used

3. Past Results – Division-Wise

Details	Target – May 2022	May 2021	May 2020	May 2019
Course Passing % – Average of 3 Divisions				
Marks Obtained by Course Topper (mark/100)				

	Division A		Division B		Division C	
Year	Initials of Teacher	% Result	Initials of Teacher	% Result	Initials of Teacher	% Result
May 2020						
May 2019						
May 2018						

4 All the Learning Resources – Books and E-Resources

4.a List of Text Books (T – Symbol for Text Books) to be Referred by Students

Sr. No	Text Book Titles	Author/s	Publisher	Edition	Module Nos.
1					
2					
3					
4					
5					

4.b List of Reference Books (R – Symbol for Reference Books) to be Referred by Students

Sr. No	Reference Book Titles	Author/s	Publisher	Edition	Module Nos.
1					
2					
3					
4					

4.c List of E - Books (E – Symbol for E-Books) to be Referred by Students

Sr. No	E- Book Titles	Author/s	Publisher	Edition	Module Nos.
1					
2					
3					
4					

4.d Reading latest / top rated research papers (at least 5 papers)

Name of Paper	Authors with Background	Published in		Problem Statement
		Date	Journal	

4.e **Based on research paper an identify the current Problem statement**

Problem Statement	Used in					
	Quiz	Assignment	Lab	Mini Project	Poster Presentation	Test

4.f **Identify Companies / Industries which use the knowledge of the subject and thus may provide Internships and final Placements**

Name of the Company	To be / Contacted for		
	Student Internship	Student Final Placement	Faculty Internship

4.g **Identify suitable relevant TOP Guest Speakers from Industry (CS50 Lecture by Mark Zuckerberg - 7 December 2005 - YouTube)**

Name of the Identified Guest Speaker	Designation	Name of the Company

4.h **Identify relevant Technical competitions to participate [Competitions -Paper Presentations, Projects, Hackathons, IVs etc..]**

Name of the Relevant Technical Competition Identified to participate	Organized by	Date of the Event

4.i **Identify faculty in TOP schools / Universities who are teaching same / similar subject and develop rapport e.g. Exchange Lecture Material (Assignments / Tests / Project etc..), Joint Paper Publication**

University	Name of the Course	Name of Faculty	Type of Collaboration		
			Exchange of Lecture Material	Joint Publication/ Research	Other

4.j **Web Links and Names of Magazines, Journals, E-journals – [VIT is member of IIT Bombay Library]**

Refer online journals subscribed in VIT library. You can also access IIT Bombay online library for journals from IITB campus.

Sr. No.	Web-Links and Names of Journals and E-Journals Recommended to Students for this Course	Web-Links and Names of Magazines Recommended to Students for this Course	Module Nos.
1			
2			
3			

4			
5			

4.k **Module Best Available in - <u>Tick ONE</u> best resource [from *<u>4.a</u>* to *<u>4.d</u>* in this AAP] & give details**

Module No.	Category (Please Tick Mark) - √						Available In VIT Library?		Details of the Resource (i.e. Name, Chapter no.etc.)
	Book			Maga-zine	Journals				
	Text	Reference	E-Book		Regular	E-Journal	Y	N	
1									
2									
3									
4									
5									
6									
7									

4.l **Referred to any top-rated university in that subject for content**

University	Name of the Course	Name of Faculty	Date of Delivery of the Course	Remarks

4.m **Faculty received any certification related to their subject. List of Certifications Identified / Done**

Course	Certifying Agency	Certification		Remarks
		Done on	Proposed to be on	

4.n **Completed subject wise/cluster wise training with cluster mentor. List of relevant Refresher Course Identified / Done**

Course	Certifying Agency (As suggested by DAB/Cluster Mentor/Industry/ University other than MU)	Certification		Remarks
		Done on	Proposed to be on	
Pedagogy				
PBL				

Sub. Content Training				

4.o Best Practices Identified and adopted

No.	Item	Best Practices Identified		
		Univ. 1	Univ. 2	Univ. 3
1	Microsite			
2	Video Lectures			
3	Assignments			
4	Mini Project			
5	Assessment Metric			
6	Quizzes			
7	Labs/ Practical (PBL)			
8	Tests			
9	Etc			
10	Peer Assessment etc.			

4.p Web Links for Online Notes/YouTube/VIT Digital Content/VIT Lecture Capture/NPTEL Videos

Students can view lectures by VIT professors, captured through LMS 'Lecture Capture' in VIT campus for previous years.

No.	Websites / Links	Module Nos.
1		
2		
3		

4.q Recommended MOOC Courses like Coursera / NPTEL / MIT-OCW / edX/VAC etc.

Sr. No.	MOOC Course Link	Course conducted by – Person / University / Institute / Industry	Course Duration	Certificate (Y / N)
1				

5 Consolidated Course Lesson Plan

	From (date/month/year)	From (date/month/year)	Total Number of Weeks
Semester Duration			

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion (Hand written)	COs Mapped	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No./ Books/ Web Site

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion (Hand written)	COs Mapped	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No./ Books/ Web Site
1							
2							
3							
4							
5							
6							
7							
8							

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion (Hand written)	COs Mapped	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No./ Books/ Web Site
9							
10							
11							
12							
13							
14							
15							
16							

6 Rubric for Grading and Marking of Term Work (inform students at the beginning of semester)

Lecture + Practical (% Attendance) & Marks	Assign-ments	Tutorial	Lab / Practical Performance	Lab Journal Assessment	Class Tests (Other than IA)	Other (1) specify	Other (2) specify	Total

7 Assignments / Tutorials Details

Assignment/ Tutorial No.	Title of the Assignments / Tutorials	CO Map	Assignment/ Tutorials given to Students on	Week of Submission
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

Analysis of Assignment / Tutorial Questions and Related Resources

Assignment / Tutorial No.	Week No.	Type* (√)			Module No.	Based on #			Question Type (√)	
		R	PQ	OBT		Text Book	Reference Book	Other Learning Resource	MU EQ	Thought Provoking
1										
2										
3										
4										
5										
6										
7										
8										
9										
10										

* Tick (√) the Type of the Assignment: Regular (R); Pop Quiz (PQ) ; Open Book Test for TE/BE/ME (OBT)
# Write number for text book, reference book, other learning resource from this AAP – *from Points 4.a to 4.d*

8 Internal Assessment / Other Class Test / Open Book Test (OBT)/Take Home Test (THT) Details

Tests	Test Dates	Module No.	CO Map	IA Question Paper Pattern	Policy
1st IA Test				Q1 – Short Questions - 10 Marks Q2 – 1 numerical 5 Marks Q3 – 1 numerical 5 Marks 20 marks each for IA 1 & 2	No IA Re-test IA is a Head of passing *
2nd IA Test					
Pop Quiz					
Open Book Test					
Take Home Test					
Class tests / prelims					
Class tests / prelims					
Any other test/exams					

*** Failures of IA test (IA1+IA2) shall appear for IA test in the next semester. There is no provision for re-test in the same semester.**

9.a Practical Activities – Regular Experiments

Practical No.	Module No.	Title of the **Regular Experiments**	Topics to be highlighted	CO Map
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

9.b Practical Activities – Newly Added Experiments

Practical No.	Module No.	Title of the **Newly Added Experiments**	Concepts to be highlighted	CO Map
1				
2				

9.c Practical Activities – PBL Experiments

Practical No.	Module No.	Title of the **PBL Experiments**	Concepts to be highlighted	CO Map
1				
2				

10 Beyond Syllabus Activities for Gap Mitigation

No.	Type of the Activity	Activities	Details – no of attendees, guest, feedback, mark sheet, report

1	**Experiential learning/Interaction with Outside World**	1- Guest Lectures by Industry Expert	
		2- Workshops	
		3- Mini Project	
		4- Industrial Visit	
		5- Any other activity	
2	**Collaborative & Group Activity**	1- Poster Presentation	
		2- Minute Papers	
		3- Students Seminars	
		4- Students Debates	
		5- Panel Discussion / Mock GD	
		6- Mock Interview	
		7- Any other activity	
3	**Co-Curricular Activity**	1- Informative videos (NPTEL/Youtube /TEDx/ MIT OW/edX)	
		2- Lecture Capture Usage	
		3- Any other activity	
4	**Tests & Assessments**	1- Class Tests/ Weekly Tests	
		2- Pop Quiz	
		3- Mobile App Based Quiz	
		4- Open Book	
		5- Take Home Test	
		6- Any other activity	

11.1 One-on-One Academic Mentoring Meetings done

No.	Name of Mentee	Date of One-On-One Meeting		
		Beginning of Sem.	After Mid Term Results	Before End Sem.

11.2 Identify Financial Concerns and refer appropriately

No.	Name of Mentee			
		Individual Goals Identified	Any Financial Concern which needs to be referred to	Any Emotional Concern to be referred to

*** Do not delete any activity. Give details for planned events. Write 'NA' for activity Not Planned.**

Consolidated Academic Administration Plan Prepared by (mention all theory teaching faculty names with signature)

Please write below your name and sign with date of the external cluster mentor meeting

Faculty 1	Faculty 2	Faculty 3

External Industry Mentor	External Academic Mentor	VIT Cluster Mentor	Program HOD

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Version 0120-7

Consolidated Academic Administration Plan for the Course Digital Design with Reconfigurable Architecture (Elective) Sem. 6 Faculty – Prof.Geeta Narayanan (Cluster Mentor) & Prof. Amaya Pethe

The academic resources available in VIT –

VMIS (ERP)	V-Refer and V-Live	VIT Library	VAC & MOOC Courses
Institute & Department Vision and Mission	Former IA question papers and solutions (prepared by faculty)	Former IA question papers solutions - hardcopy	Value Added Courses (VAC) are conducted throughout the semester & in the semester break - Enrol for the VACs
Program Educational Objectives (PEO)	MU end semester examination question papers and solutions (prepared by faculty)	MU end semester exam question paper & solutions - by faculty, hardcopy	
Program Specific Outcome (PSO)	Class notes and Digital Content for the subject (scanned / typed by faculty)	All text books, reference books, e -books mentioned in the syllabus & AAP	Online courses from NPTEL, Coursera etc. are pursued throughout the semester - Register for the course & get certified
Program Outcome (PO)	Comprehensive question bank, EQ, GQ, PPT, Class Test papers	Technical journals and magazines for reference	
Departmental Knowledge Map	Academic Administration Plan & Beyond Syllabus Activity report	VIT library is member of IIT Bombay Library	Watch former lectures captured in LMS at VIT

1.a Course Objectives (Write in detail – as per NBA guidelines)

Cognitive	What do you want students to know?	To understand, analyze & design finite state machines (FSM) To prepare students to design FSM using hardware description languages (HDL)
Affective	What do you want students to think / care about?	To motivate students to use reconfigurable devices for digital systems
Behavioural	What do you want students to be able to do?	To train students in writing VHDL code of combinational & sequential circuits

Advice to Students:

Attend every class!!! Missing even one class can have a substantial effect on your ability to understand the course. Be prepared to think and concentrate, in the class and outside. I will try to make the class very interactive. Participate in the class discussions. Ask questions when you don't understand something. Keep up with the class readings. Start assignments and homework early. Meet me in office hour to discuss ideas, solutions or to check if what you understand is correct. The v-Refer Link for this course (**Creation of microsite (vit.edu.in or teams) e.g. https://cs50.harvard.edu/college/2021/spring/)**

Collaboration Policy:

We encourage discussion between students regarding the course material. However, no discussion of any sort is allowed with anyone on the assignment and homework for the class. If you find solution to some problems in a book or on the internet, you may use their idea for the solution; provided you acknowledge the source (name and page in the book or the website, if the idea is found on the internet). Even though you are allowed to use ideas from another source, you must write the solution in your own words. If you are unsure whether or not certain kinds of collaboration is possible please ask the teacher.

1.b Course Outcome (CO) Statements and Module-Wise Mapping (follow NBA guideline)

CO No.	Statements	Related Module/s
CO601.1	Analyze & design FSM.	1,4
CO601.2	Understand fundamentals of HDL and its use for designing combinational circuits.	2
CO601.3	Apply the concept of HDL for designing sequential circuits.	3,4
CO601.4	Develop FSM by using the fundamentals of HDL.	1,2,3,4
CO601.5	Design of complex digital systems.	5
CO601.6	Understand and distinguish FPGA and CPLD architecture.	6

1.c Mapping of COs with POs (mark S: Strong, M: Moderate, W: Weak, Dash '–': not mapped)

(List of POs is available in V-refer)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	S	S	S	M	S	W	--	--	M	--	--	S
CO 2	S	S	S	W	S	M	--	--	M	--	--	S
CO 3	S	S	S	M	S	W	--	--	M	--	W	S
CO 4	S	S	S	M	M	W	--	--	S	--	--	S
CO 5	S	S	S	M	S	W	--	--	W	--	S	S
CO 6	--	M	--	--	S	W	--	--	W	--	--	S

1.d Mapping of COs with PSOs (mark S: Strong, M: Moderate, W: Weak, Dash '–':not mapped)

	PSO 1	PSO 2	PSO 3
CO 1	S	S	M
CO 2	S	M	M
CO 3	S	S	M
CO 4	S	S	M
CO 5	S	S	M
CO 6	S	S	--

1.e Teaching and Examination Scheme (As specified by the University) for the Course

Categories	Mathematics	Basic Science & General Engg.	Humanities & Soft Skill	Core Engg./ Technology - Design & Analysis	Multidisciplinary
Tick suitable category				√	

Subject Code	Subject Name	Teaching Scheme			Credits Assigned			
		Theory	Practical	Tutorial	Theory	TW/Practical	Tutorial	Total
ELDO601	Digital Design with Reconfigurable Architecture	03	--	--	03	--	--	03
--		--	--	--	--	--	--	--

Subject Code	Subject Name	Examination Scheme							
		Theory Marks IA Test			End Sem. Exam Marks	TW	Practical	Oral	Total
		IA 1	IA 2	Average of IA1 and IA2					
ELDO601	Digital Design with Reconfigurable Architecture	20	20	20	80	--	--	--	--
--	--	--	--	--	--	--	--	--	--

1.f Faculty-Wise Distribution of all Lecture-Practical-Tutorial Hours for the Course

Divisions	Lecture (Hrs.)	Practical (Hrs.)				Tutorial (Hrs.)			
		Batch 1	Batch 2	Batch 3	Batch 4	Batch 1	Batch 2	Batch 3	Batch 4
A	--	--	--	--	--	--	--	--	--
B	--	--	--	--	--	--	--	--	--
C	--	--	--	--	--	--	--	--	--

1.g Office Hours (Faculty will be available in office in this duration for solving students' query)

Division	Day	Time (at least 1 Hr. / Division)	Venue (Office Room No.)
A	Thuday	4.00 pm to 5.00 pm	L-014
B			
C			

2.a Syllabus : Module Wise Teaching Hours and % Weightage in University Question Paper

Module No.	Module Title and Brief Details	Teaching Hrs. for each module	% Weightage in University Question Papers
1	State Machines Design	8	21
2	Introduction to VHDL	8	21
3	Design of sequential circuit using VHDL	6	15
4	Design of Finite State Machines (FSM) using VHDL	6	15
5	System Design using VHDL	6	15
6	Simulation, Synthesis and Implementation	5	13
* Insert rows for more modules in the Course	**Total**	**39**	**100**

2.b Prerequisite Courses

No.	Semester	Name of the Course	Topic/s
1	3	Digital Logic Circuits	1,2,3,5
2			
3			

2.c Relevance to Future Courses

No.	Semester	Name of the Course
1	8	Analog and Mixed VLSI
2		
3		

2.d Identify real life scenarios / examples which use the knowledge of the subject

Real Life Scenario	Concept Used
Vending Machine	Finite State Machines
Traffic Light Controller	Finite State Machines, VHDL
ALU Design	VHDL

3. Past Results – Division-Wise

Details	Target – May 2022	May 2021	May 2020	May 2019
Course Passing % – Average of 3 Divisions	100	--	--	--
Marks Obtained by Course Topper (mark/100)	--	--	--	--

	Division A		Division B		Division C	
Year	Initials of Teacher	% Result	Initials of Teacher	% Result	Initials of Teacher	% Result
May 2020	--	--	--	--	--	--
May 2019	--	--	--	--	--	--
May 2018	--	--	--	--	--	--

4 All the Learning Resources – Books and E-Resources

4.a List of Text Books (T – Symbol for Text Books) to be Referred by Students

Sr. No	Text Book Titles	Author/s	Publisher	Edition	Module Nos.
1	Digital Design	M. Morris Mano	Pearson Education India, 2012.	5th Edition	1
2	Digital Design Principles & Practices	John Wakerley	Pearson Publication	3rd edition	1,2,5,6
3	Circuit Design with VHDL	Volnei A. Pedroni	MIT Press	3rd edition	2,3,4,5
4	FPGA Based System Design	Wayne Wolf	Pearson Education.	3rd edition	6
5	Engineering Approach to Digital Design	W. I. Fletcher	PHI publications	3rd edition	5,6

4.b List of Reference Books (R – Symbol for Reference Books) to be Referred by Students

Sr. No	Reference Book Titles	Author/s	Publisher	Edition	Module Nos.
1	Modern Digital Electronics	R. P. Jain	McGraw Hill Education	4th Edition	1
2	Fundamentals of Digital Logic Design	Stephen Brown, Zvonko Vranesic	McGrawHill	2nd edition	1,5,6
3	Digital Logic Applications and Design	John M. Yarbrough	Thomson Publications	2nd edition	1
4	The students guide to VHDL.	P. J. Ashenden	Elsevier,1999	2nd edition	2,3,4,5

5	Xilinx online resources – www.xilnix.com	--	--	--	2,3,4,5

4.c List of E - Books (E – Symbol for E-Books) to be Referred by Students

Sr. No	E- Book Titles	Author/s	Publisher	Edition	Module Nos.
1	Circuit Design with VHDL	Volnei A. Pedroni	MIT Press	3rd edition	2,3,4,5
2					
3					
4					

4.d Reading latest / top rated research papers (at least 5 papers)

Name of Paper	Authors with Background	Published in		Problem Statement
		Date	Journal	
A Low Area High Speed FPGA Implementation of AES Architecture for Cryptography Application https://www.mdpi.com/2079-9292/10/16/2023	Thanikodi Manoj kumar, Kasarala Satish Reddy, Stefano Renaldy, Bidare Parameshchari, Kavitha Arunachalam	21 August2021	Electronics 2021 Journal	This research article details the low power high-speed hardware architectures for the efficient field programmable gate array (FPGA) implementation of the advanced encryption standard (AES) algorithm to provide data security
A Concept of Visual Programming Tool for Learning VHDL https://iopscience.iop.org/article/10.1088/1757-899X/1031/1/012120/meta	Aneliya Ivanova	4th-6th November 2020	IOP Conference Series: Materials Science and Engineering, Volume 1031, International Conference on Technics, Technologies and Education 2020 (ICTTE 2020), Yambol, Bulgaria	Due to the COVID-19 pandemic, distance education starts playing a crucial role in higher education and the need for development of educational tools, helping the students learn better at home cannot be ignored. Teaching programming languages online is a complicated task and when the course subject is programmable logic design through Hardware Description Languages (HDLs), online teaching becomes a complex challenge. In this paper is presented a concept of a training environment that uses the visual programming technique to help the students

				create VHDL models of various digital devices.
A Proposal of FPGA-based Low Cost and Power Efficient Autonomous Fruit Harvester https://patelmanthan.in/wp-content/uploads/2020/01/ICCAR_2020.pdf	Kumar Nilay, Swarnabha Mandal, Yash Agarwal, Rishabh Gupta, Sumeet Kumar, Poojan Shah, Sombit Dey, Manthan Patel, Annanya	20-23 April 2020	International Conference on control,Automation and Robotics (ICCAR)	A power-efficient and low-cost prototype of a robotic harvester which employs multiple subsystems such as fruit detection, odometry, localization, proficient manipulation through computer vision, deep learning and A novel end-effector design. Fruit Plucking is performed using an end effector, and 3-degree of freedom (DOF) arm (made out of the integration of two linear actuators and a rotating platform) consolidated with a 4-wheeled differential drive mobile platform. Effective implementation of the visual processing is executed on the FPGA Fabric of the Xilinx PYNQ-Z2 Board, which accelerates Deep Neural Networks (DNNs) with improved Latency and Energy Ef
Implementation of digital and analog modulation systems using FPGA http://ijeecs.iaescore.com/index.php/IJEECS/article/view/19033	Raya. K Mohammed, Hamsa A. Abdullah	April 2020	Indonesian Journal of Electrical Engineering and Computer Science (IJEECS)	FPGA (Field Programmable Gate Array) based implementations of digital and analog modulation techniques play a vital rule in the design of signal processing system. The performance and flexibility provided by reconfigurable computing speeds up the development process in signal processing implementations using FPGA. Different methods for digital and analog modulation are designed in this paper by using System Generator tools & Vivado.
Pass Transistor Adiabatic Logic with NMOS pull-down configuration in stand-by mode https://ieeexplore.ieee.org/document/786	Prasad Khandekar Ketan Raut Uday Khambete Pallavi Vane	12-13 August 2016	International Conference on Computing Communication Control and automation (ICCUBEA)	This paper presents design of 2:1 MUX using adiabatic logic style PAL2NSM and the results of energy dissipation are compared with simple CMOS 2:1 MUX.

0123				

4.e **Based on research paper an identify the current Problem statement**

Problem Statement	Used in					
	Quiz	Assignment	Lab	Mini Project	Poster Presentation	Test
The students construct VHDL models by combining simple visual objects while the environment is providing guidance in real time				√		

4.f **Identify Companies / Industries which use the knowledge of the subject and thus may provide Internships and final Placements**

Name of the Company	To be / Contacted for		
	Student Internship	Student Final Placement	Faculty Internship
Semiconductor Laboratory (SCL-student training), Department of Space, Government of India http://www.scl.gov.in/student%20training.html	√		

4.g **Identify suitable relevant TOP Guest Speakers from Industry (CS50 Lecture by Mark Zuckerberg - 7 December 2005 - YouTube)**

Name of the Identified Guest Speaker	Designation	Name of the Company
Mr. Uday Khambete	Scientist	SCL

4.h **Identify relevant Technical competitions to participate [Competitions -Paper Presentations, Projects, Hackathons, IVs etc..]**

Name of the Relevant Technical Competition Identified to participate	Organized by	Date of the Event
35th International Conference on VLSI Design https://vlsid.org/	VLSID 2022 Design Contest	26th February to 2nd March 2022
Smart India Hackathon (SIH-2022) https://www.sih.gov.in/sih2022	AICTE,MHRD innovation cell, Persistent ,Ministry Of	Registration through college SPOC by 31st March 2022. Event dates: April 2022

	Education, Government of India	

4.i **Identify faculty in TOP schools / Universities who are teaching same / similar subject and develop rapport e.g. Exchange Lecture Material (Assignments / Tests / Project etc..), Joint Paper Publication**

University	Name of the Course	Name of Faculty	Type of Collaboration		
			Exchange of Lecture Material	Joint Publication/ Research	Other
NIT, Rurkela	EC6203 : Reconfigurable System Design	Prof. Debiprasad Priyabrata Acharya	√		

4.j **Web Links and Names of Magazines, Journals, E-journals – [VIT is member of IIT Bombay Library]**

Refer online journals subscribed in VIT library. You can also access IIT Bombay online library for journals from IITB campus.

Sr. No.	Web-Links and Names of Journals and E-Journals Recommended to Students for this Course	Web-Links and Names of Magazines Recommended to Students for this Course	Module Nos.
1	MITcoursewarehttps://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-002-circuits-and-electronics-spring-2007/	IEEE Spectrum	All Modules
2	***nptel***.*iitm.ac.in*	Electronics For You	All Modules
3	IEEE Transactions on Electron Devices	IEEE industrial Electronics Magazine	All Modules
4	IEEE Electron Device Letters	IEEE Electronics Online e-magazine	All Modules
5			

4.k **Module Best Available in - <u>Tick ONE</u> best resource [from *<u>4.a</u>* to *<u>4.d</u>* in this AAP] & give details**

Module No.	Category (Please Tick Mark) - √						Available In VIT Library?		Details of the Resource (i.e. Name, Chapter no.etc.)
	Book			Maga-zine	Journals		Y	N	
	Text	Reference	E-Book		Regular	E-Journal			
1	√						√		Digital Logic and Computer Design,Morris Mano Ch No 6
2	√						√		Circuit Design with VHDL,Pedroni ch no.2-6
3	√						√		Circuit Design with VHDL,Pedroni ch no.7-8
4	√						√		Circuit Design with VHDL,Pedroni ch no.9

5	√						√		Circuit Design with VHDL,Pedroni ch no.10-12
6	√						√		Digital Logic and Computer Design,Morris Mano Ch No 8

4.l **Referred to any top-rated university in that subject for content**

University	Name of the Course	Name of Faculty	Date of Delivery of the Course	Remarks
Cankaya University, Ankara-Turkey	VHDL Circuit Design, Simulation and FPGA Programming Using VIVADO	Speaker: Orhan Gazi,	Web-based Course with live Instructor! Times & Dates: 11AM - 12 noon ET, February 15, 17, 22, 24, March 1, 3, 8, 10, 15, 17	IEEE,Boston

4.m **Faculty received any certification related to their subject. List of Certifications Identified / Done**

Course	Certifying Agency	Certification		Remarks
		Done on	Proposed to be on	
Swithing Circuits and Logic Design	NPTEL-AICTE	July-October 2018	--	74%
Hardware Modelling using Verilog	NPTEL	Sept-Nov 2020	--	60%

4.n **Completed subject wise/cluster wise training with cluster mentor. List of relevant Refresher Course Identified / Done**

Course	Certifying Agency (As suggested by DAB/Cluster Mentor/Industry/ University other than MU)	Certification		Remarks
		Done on	Proposed to be on	
Pedagogy	VIT,IEEE	21-25 June 2020	--	One-week FDP on "Modern Educational tools and Pedagogical Practices for Online Teaching
PBL	ATAL Academy	7-12 Dec 2020		Design Thinking
Sub.	NPTEL-AICTE	Jul-Oct 2018		Swithing Circuits and Logic Design

Content Training	NPTEL	Sept-Nov 2020		Hardware Modelling using Verilog

4.o Best Practices Identified and adopted

No.	Item	Best Practices Identified		
		Univ. 1	Univ. 2	Univ. 3
1	Microsite	Cadence and Xilinx Introduce FPGA IP Ecosystem Microsite		
2	Video Lectures			
3	Assignments		Individual Assignment, Rochester Institute of Technology (RIT) https://www.se.rit.edu/~se463/Co-Design/IndividualVHDL.html	
4	Mini Project	Design examples, University of Kent		
5	Assessment Metric			
6	Quizzes			VHDL whiz https://vhdlwhiz.com/author/bigkahuna/ VHDLwhiz helps to understand advanced concepts within FPGA design without being overly technical.
7	Labs/ Practical (PBL)			
8	Tests			
9	Etc			
10	Peer Assessment etc.			

4.p Web Links for Online Notes/YouTube/VIT Digital Content/VIT Lecture Capture/NPTEL Videos

Students can view lectures by VIT professors, captured through LMS 'Lecture Capture' in VIT campus for previous years.

No.	Websites / Links	Module Nos.
1	https://nptel.ac.in/courses/117/108/117108040/	All
2	https://www.youtube.com/watch?v=BDq8-QDXmek	2
3	https://www.youtube.com/watch?v=S230ViKmXQc	3,4

4.q Recommended MOOC Courses like Coursera / NPTEL / MIT-OCW / edX/VAC etc.

Sr. No.	MOOC Course Link	Course conducted by – Person / University / Institute / Industry	Course Duration	Certificate (Y / N)

1	https://onlinecourses.nptel.ac.in/noc22_ee45/preview	Dr. Neeraj Goel, IIT, ROPAR	12 Week	Y

5 Consolidated Course Lesson Plan

	From (date/month/year)	From (date/month/year)	Total Number of Weeks
Semester Duration	10/01/2022	30/04/2022	15

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion (Hand written)	COs Mapped	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No./ Books/ Web Site
1	1,2,3	1	Mealy and Moore machines, clocked synchronous state machine design, state reduction techniques, State assignment,		601.1		Digital Logic and Computer DesignMorris Mano
2	4,5,6	1	Clocked synchronous state machine analysis. Design examples on overlapping and non-overlapping sequence detector, Odd/even parity checker for serial data,		601.1		Digital Logic and Computer DesignMorris Mano
3	7,8,9	1, 2	vending machines.		601.1,2		Digital Design John Wakerly
4	10,11,12	2	Core features of VHDL, Data types, Concurrent and Sequential statements, Data flow, Behavioural and Structural architectures, Subprograms:		601.2		Circuit Design with VHDL

Week	Lecture no.	Module No.	Lecture Topics / IA 1 and IA 2 / BSA planned to be covered	Actual date of Completion (Hand written)	COs Mapped	Recommended Prior Viewing / Reading	
						Lecture No. (on LMS)	Chapter No./ Books/ Web Site
5	13,14,15	2	Function and Procedure, Design examples of combinational circuits like Multiplexers, De-multiplexers, Adder, Subtractor		601.2		Circuit Design with VHDL
6	16,17,18	2,3	Priority Encoder Design examples for Flip flops		601.2,3		Circuit Design with VHDL
7	19,20,21	3	Synchronous counters, Asynchronous counters,		601.3		Circuit Design with VHDL
8	22,23,24	3,4	Shift registers VHDL code for Moore, Mealy type FSMs,		601.3,4		Circuit Design with VHDL
9	25,26,27	4	Serial adders, Traffic light controller,		601.4		Circuit Design with VHDL
10	28,29,30	4,5	Vending machines Parallel Multiplication		601.4,5		Circuit Design with VHDL
11	31,32,33	5	Booth Multiplication, MAC unit,		601.5		Circuit Design with VHDL
12	34,35,36	5,6	ALU, Memory: ROM and RAM, Functional simulation, Timing simulation		601.5,6		Circuit Design with VHDL
13	37,38,39	6	Logic synthesis, RTL.CPLD, SRAM based FPGA architecture, Spartan II.		601.6		Digital Logic and Computer DesignMorris Mano

6 Rubric for Grading and Marking of Term Work (inform students at the beginning of semester)

Lecture + Practical (% Attendance) & Marks	Assign-ments	Tutorial	Lab / Practical Performance	Lab Journal Assessment	Class Tests (Other than IA)	Other (1) specify	Other (2) specify	Total
--	--	--	--	--	--	--	--	--

7 Assignments / Tutorials Details

Assignment/ Tutorial No.	Title of the Assignments / Tutorials	CO Map	Assignment/ Tutorials given to Students on	Week of Submission
1	State Machines Design	CO601.1	Week 2	Week 4
2	Introduction to VHDL	CO601.2	Week 4	Week 6
3	Design of sequential circuit using VHDL	CO601.3	Week 6	Week 8
4	Design of Finite State Machines (FSM) using VHDL	CO601.4	Week 8	Week 10
5	System Design using VHDL	CO601.5	Week 10	Week 11
6	Simulation, Synthesis and Implementation	CO601.6	Week 11	Week 12
7				
8				
9				
10				

Analysis of Assignment / Tutorial Questions and Related Resources

Assignment / Tutorial No.	Week No.	Type* (√)			Module No.	Based on #			Question Type (√)	
		R	PQ	OBT		Text Book	Reference Book	Other Learning Resource	MU EQ	Thought Provoking
1	2	√	√		1	1,2	1			√
2	4	√	√		2	2	3			√
3	6	√			3	2	3			√
4	8	√			4	2	3			√
5	10				5	2	3			√
6	11				6	1,2				√
7										
8										
9										
10										

* Tick (√) the Type of the Assignment: Regular (R); Pop Quiz (PQ) ; Open Book Test for TE/BE/ME (OBT)
# Write number for text book, reference book, other learning resource from this AAP – *from Points 4.a to 4.d*

8 Internal Assessment / Other Class Test / Open Book Test (OBT)/Take Home Test (THT) Details

Tests	Test Dates	Module No.	CO Map	IA Question Paper Pattern	Policy
1st IA Test		1,2	CO601.1 CO601.2	Q1 – Short Questions - 10 Marks Q2 – 1 numerical 5 Marks Q3 – 1 numerical 5 Marks 20 marks each for IA 1 & 2	No IA Re-test IA is a Head of passing *
2nd IA Test		3,4,5,6	CO601.3 CO601.4 CO601.5 CO601.6		
Pop Quiz					
Open Book Test					
Take Home Test					
Class tests / prelims					

Class tests / prelims					
Any other test/exams					

*** Failures of IA test (IA1+IA2) shall appear for IA test in the next semester. There is no provision for re-test in the same semester.**

9.a Practical Activities – Regular Experiments

Practical No.	Module No.	Title of the **Regular Experiments**	Topics to be highlighted	CO Map
1	--	--	--	--
2	--	--	--	--
3	--	--	--	--
4	--	--	--	--
5	--	--	--	--
6	--	--	--	--
7	--	--	--	--
8	--	--	--	--
9	--	--	--	--
10	--	--	--	--

9.b Practical Activities – Newly Added Experiments

Practical No.	Module No.	Title of the **Newly Added Experiments**	Concepts to be highlighted	CO Map
1	--	--	--	--
2	--	--	--	--

9.c Practical Activities – PBL Experiments

Practical No.	Module No.	Title of the **PBL Experiments**	Concepts to be highlighted	CO Map
1	--	--	--	--

2	--	--	--	--

10 Beyond Syllabus Activities for Gap Mitigation

No.	Type of the Activity	Activities	Details – no of attendees, guest, feedback, mark sheet, report
1	**Experiential learning/Interaction with Outside World**	1- Guest Lectures by Industry Expert	YES (Mr. Uday Khambete, SCL)
		2- Workshops	NA
		3- Mini Project	YES
		4- Industrial Visit	NA
		5- Any other activity	Few hands-on sessions on EDA playground
2	**Collaborative & Group Activity**	1- Poster Presentation	NA
		2- Minute Papers	NA
		3- Students Seminars	YES
		4- Students Debates	NA
		5- Panel Discussion / Mock GD	NA
		6- Mock Interview	NA
		7- Any other activity	NA
3	**Co-Curricular Activity**	1- Informative videos (NPTEL/Youtube /TEDx/ MIT OW/edX)	YES
		2- Lecture Capture Usage	NA
		3- Any other activity	
4	**Tests & Assessments**	1- Class Tests/ Weekly Tests	YES
		2- Pop Quiz	YES
		3- Mobile App Based Quiz	NA
		4- Open Book	YES

		5- Take Home Test	NA
		6- Any other activity	NA

11.1 One-on-One Academic Mentoring Meetings done

No.	Name of Mentee	Date of One-On-One Meeting		
		Beginning of Sem.	After Mid Term Results	Before End Sem.

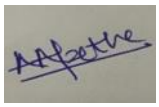
11.2 Identify Financial Concerns and refer appropriately

No.	Name of Mentee			
		Individual Goals Identified	Any Financial Concern which needs to be referred to	Any Emotional Concern to be referred to

*** Do not delete any activity. Give details for planned events. Write 'NA' for activity Not Planned.**

Consolidated Academic Administration Plan Prepared by (mention all theory teaching faculty names with signature)

Please write below your name and sign with date of the external cluster mentor meeting

 Faculty 1	Faculty 2	Faculty 3

External Industry Mentor	External Academic Mentor	 VIT Cluster Mentor	 Program HOD